

Fig. 1

10033446-122701

Branch is approved

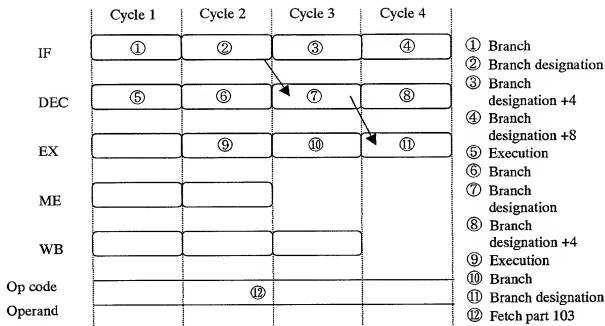


Fig. 2 A

Branch is not approved

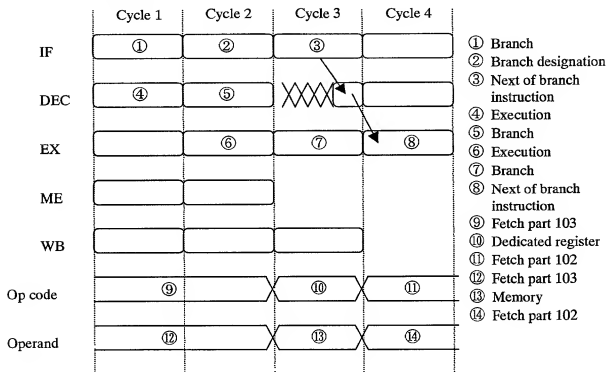


Fig. 2 B

10033446.122701

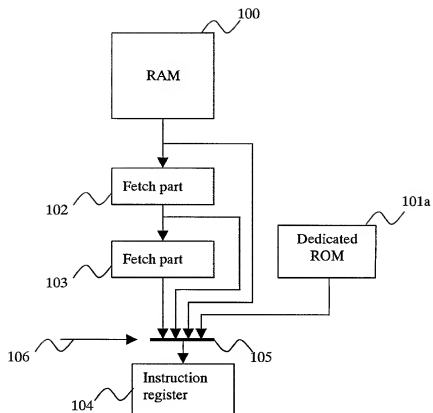


Fig. 3

10033446.122701

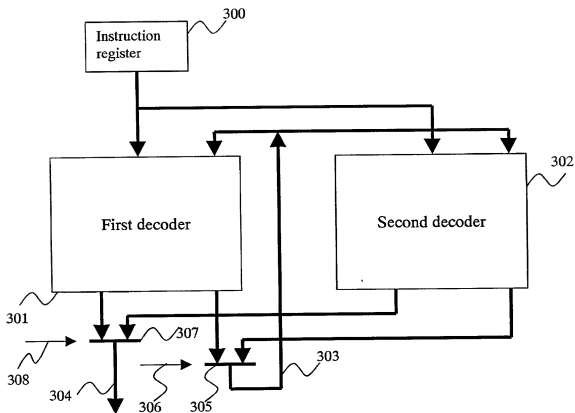


Fig. 4

1003446-122701

Branch is approved

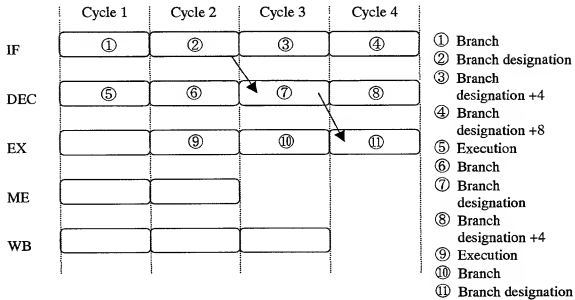


Fig. 5 A

Branch is not approved

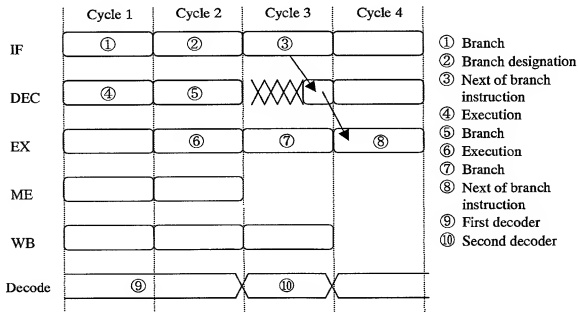


Fig. 5 B

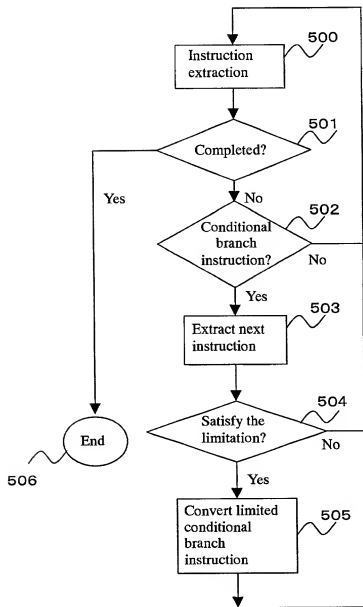


Fig. 6

10033446-122704

Example of case statement	Assembler description	Converted result of instruction sequence
switch(mode)	ld d0,(mode)	ld d0,(mode)
case: 1 a=b+1;	cmp d0,1	cmp d0,1
case: 3 a=c;	jz	cjz
case: 5 a=b+c;	cmp d0,3	cmp d0,3
:	jz	cjz
:	cmp d0,5	cmp d0,5
	jz	cjz
	:	:
	:	:
Fig. 7A	Fig. 7B	Fig. 7C

10033446.122701

Branch is approved

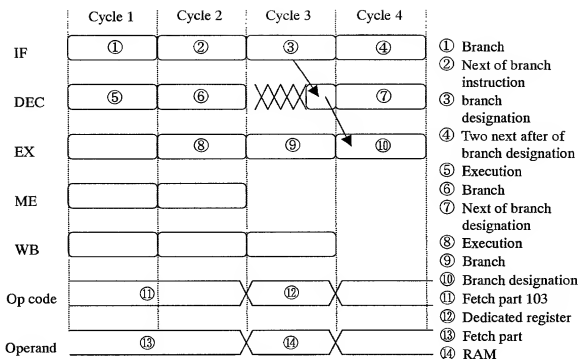


Fig. 8 A

Branch is not approved

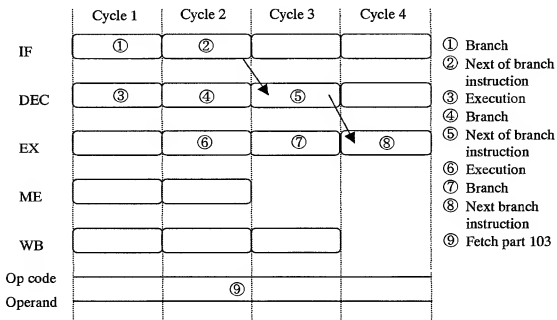


Fig. 8 B

10033446-122701



Branch is approved

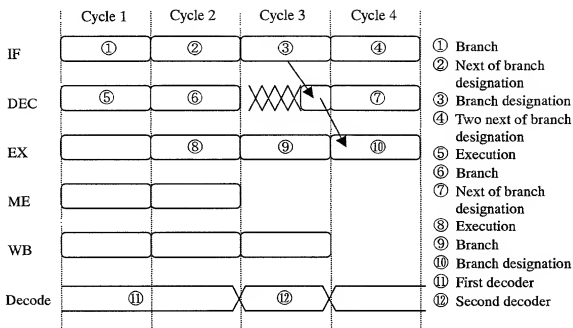


Fig. 9 A

Branch is not approved

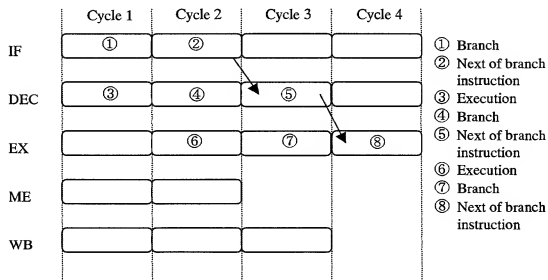


Fig. 9 B

10033446-122701

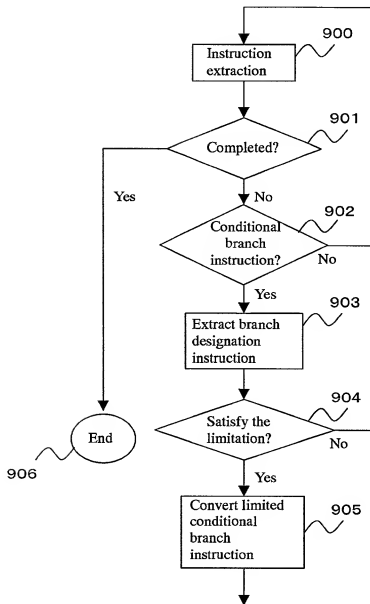


Fig. 10

Example of case statement	Assembler description	Converted result of instruction sequence
switch(mode)	ld d0,(mode)	ld d0,(mode)
case: 1 a=b+1;	cmp d0,1	cmp d0,1
case: 3 a=c;	jnz A	cjnz A
case: 5 a=b+c;	ld d0,(b)	ld d0,(b)
:	add d0,1	add d0,1
:	st d0,(a)	st d0,(a)
	jmp END	jmp END
Fig. 11A	A: cmp d0,3	A: cmp d0,3
	jnz B	cjnz B
	ld d0,(c)	ld d0,(c)
	st d0,(a)	st d0,(a)
	jmp END	jmp END
	B: cmp d0,5	B: cmp d0,5
	jnz C	cjnz C
	ld d0,(c)	ld d0,(c)
	ld d1,(b)	ld d1,(b)
	add d0,d1	add d0,d1
	st d0,(a)	st d0,(a)
	:	:
	:	:
	END:	END:

Fig. 11B

Fig. 11C

10034445-122701

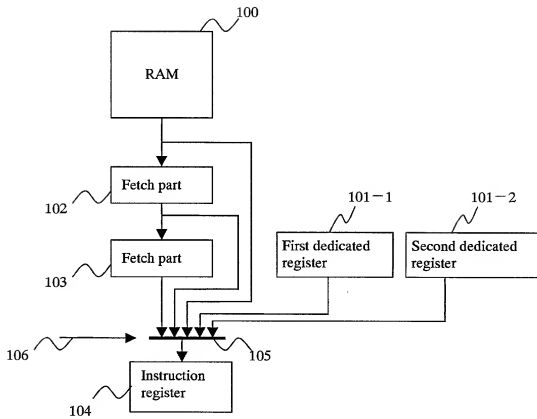


Fig. 12

# Unconditional branch

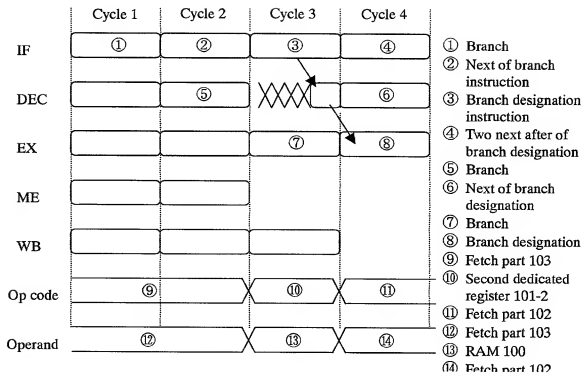


Fig. 13

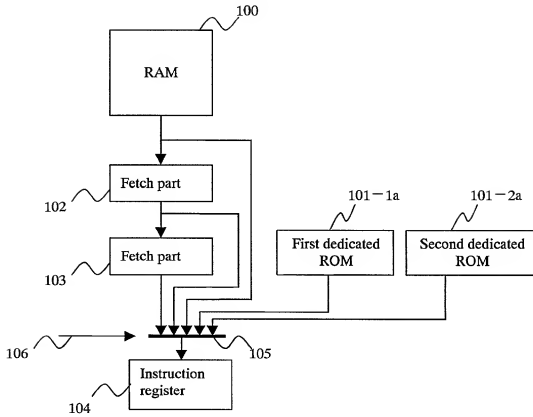


Fig. 14

# Unconditional branch

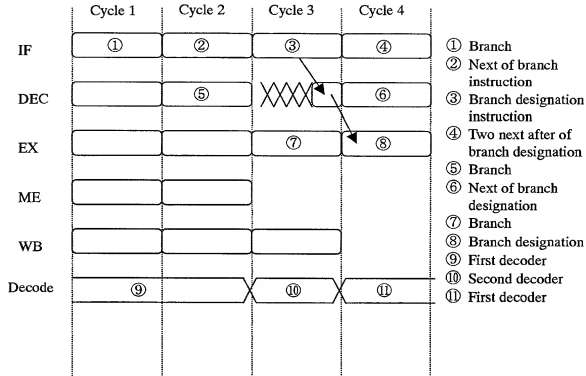


Fig. 15

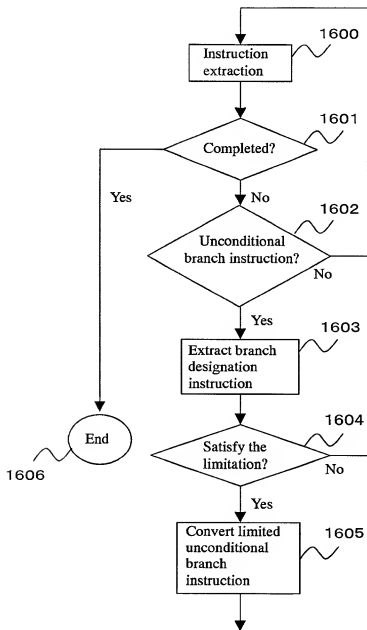


Fig. 16



### Example of case statement

```
switch(mode1){  
    case: 1 a1=b1+1;  
    case: 3 a1=c1;  
    case: 5 a1=b1+c1;  
}  
switch(mode2){  
    case: 1 a2=b2+1;  
    case: 3 a2=c2;  
    case: 5 a2=b2+c2;  
}
```

Fig. 17

10033446-122701

# Assembler description

ld d0,(mode1)	C1 ld d0,(mode2)
cmp d0,1	cmp d0,1
jnz A1	jnz A2
ld d0,(b)	ld d0,(b)
add d0,1	add d0,1
st d0,(a)	st d0,(a)
jmp C1	jmp C2
A1: cmp d0,3	A1: cmp d0,3
jnz B1	jnz B2
ld d0,(c)	ld d0,(c)
st d0,(a)	st d0,(a)
jmp C1	jmp C2
B1: cmp d0,5	B1: cmp d0,5
jnz C1	jnz C2
ld d0,(c)	ld d0,(c)
ld d1,(b)	ld d1,(b)
add d0,d1	add d0,d1
st d0,(a)	st d0,(a)
	C2: . . .
	. . .

Fig. 18

# Instruction sequence after conversion

ld d0,(mode1)	C1	ld d0,(mode2)
cmp d0,1		cmp d0,1
cjnz A1		cjnz A2
ld d0,(b)		ld d0,(b)
add d0,1		add d0,1
st d0,(a)		st d0,(a)
cjmp C1		cjmp C2
A1: cmp d0,3	A1:	cmp d0,3
cjnz B1		cjnz B2
ld d0,(c)		ld d0,(c)
st d0,(a)		st d0,(a)
cjmp C1		cjmp C2
B1: cmp d0,5	B1:	cmp d0,5
cjnz C1		cjnz C2
ld d0,(c)		ld d0,(c)
ld d1,(b)		ld d1,(b)
add d0,d1		add d0,d1
st d0,(a)		st d0,(a)
	C2:	. . .
		. . .

Fig. 19

Branch is approved

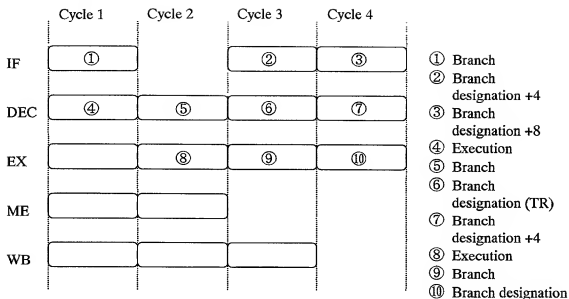


Fig. 20 A PRIOR ART

Branch is not approved

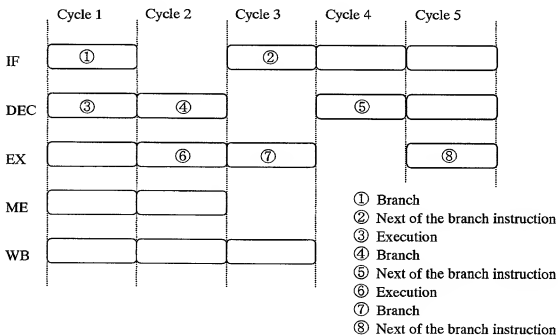


Fig. 20 B PRIOR ART

10033446-122701

Branch is approved

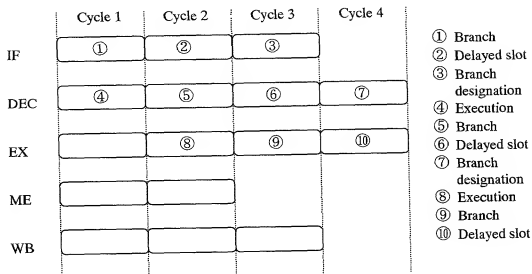


Fig. 21 A PRIOR ART

Branch is not approved

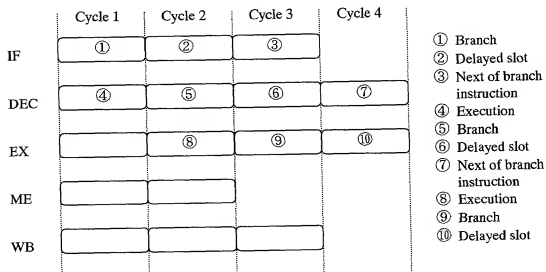


Fig. 21 B PRIOR ART

1003446.12221

Example of  
case statement

```
switch(mode)
case: 1 a=b+1;
case: 3 a=c;
case: 5 a=b+c;
:
:
```

Fig. 22A

PRIOR ART

Assembler  
description

```
ld d0,(mode)
cmp d0,1
jz
cmp d0,3
jz
cmp d0,5
jz
:
:
```

Fig. 22B

PRIOR ART

1003446-122701